

A method of testing an integrated circuit

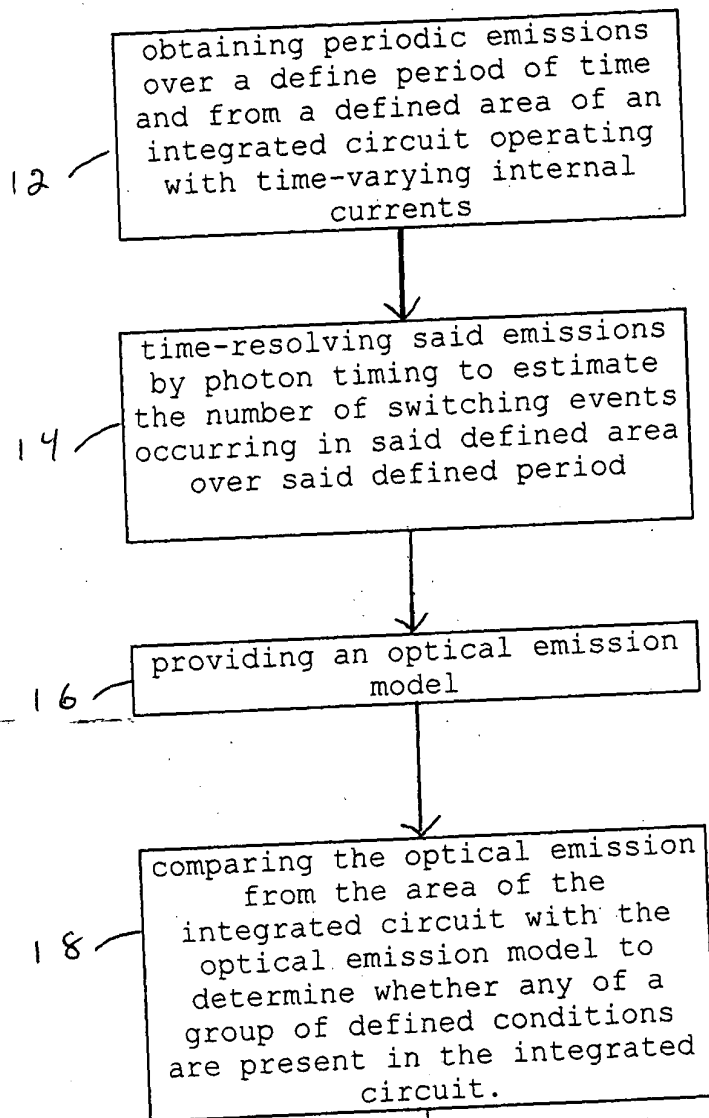


Figure 1

20200920 984200T 1007486 020702

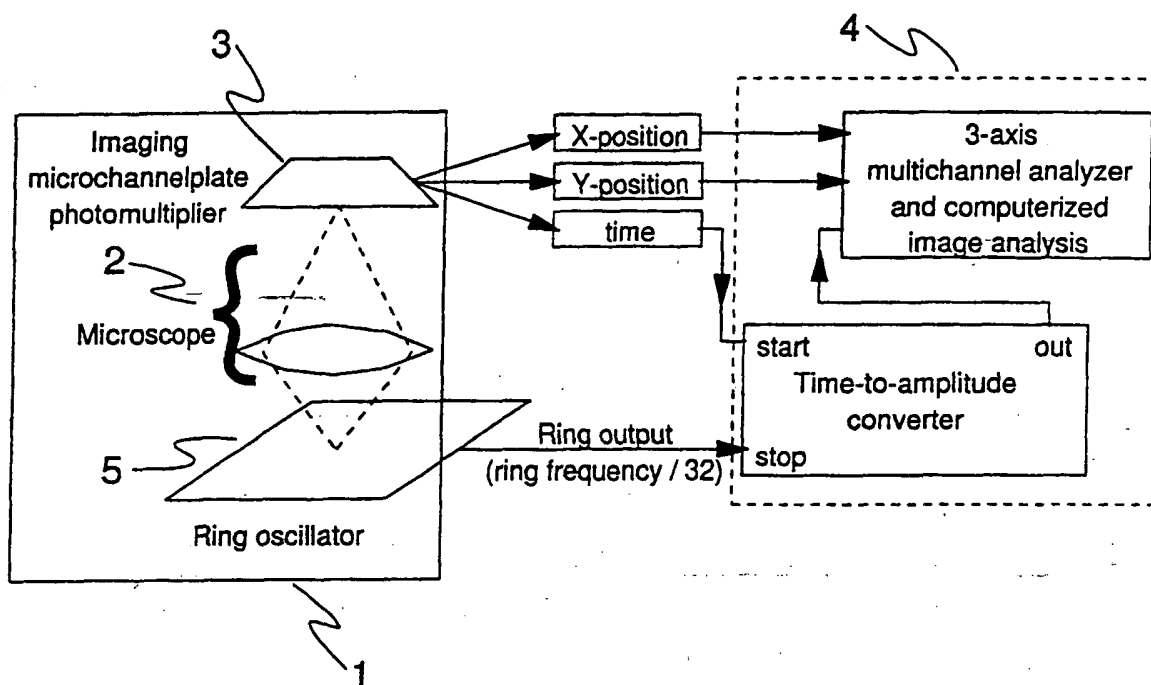


Figure 2